

Overview

This IP is a low-power, 8-bit synchronous differential voltage ADC with integrated sample-and-hold and power-down features. It supports ~ 1 V peak-to-peak input swing around a $0.5 \times V_{DD}$ common-mode voltage and includes an optional serialized digital output. The synchronous architecture enables dynamic reduction of digital power in steady-state conditions. Designed in 65 nm technology, it achieves ~ 7.5 ENOB with ~ 1.1 μA current consumption and a 25 kHz input bandwidth.

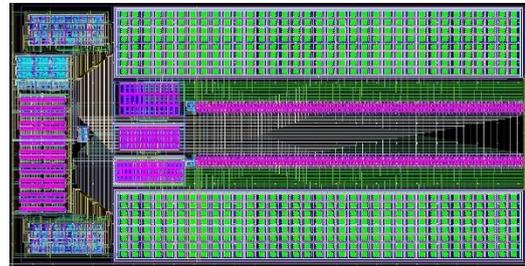
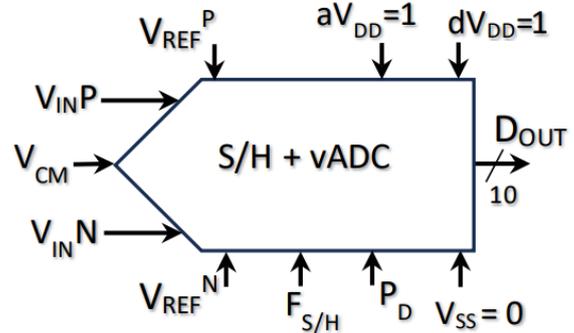
Key Features

- 8-bit resolution, Low-Power, Differential voltage-input, Synchronous vADC with S/H & Power Down
- Optional: Digital output port (D_{OUT}) can be serialized as needed.
- Digital power consumption reduces dynamically in steady-state V_{IN} conditions, enabled by synchronous vADC architecture.
- V_{INP} and V_{INN} terminals swing $\sim 1\text{V}$ Peak-to-Peak around common mode voltage (e.g., $V_{CM} \approx 0.5 \times V_{DD}$)
- Example: $V_{REFP} \approx 1\text{v}$ and $V_{REFN} \approx 0\text{v}$

Applications

- Wearable devices
- Audio applications

Block Diagram



Specifications

Resolution [Bits]	8
$V_{REF P}$ [V]	~ 1
$V_{REF N}$ [V]	0
V_{CM} [V]	$\sim 0.5 \times V_{DD}$
I_{DD} [μA]	~ 1.1
ENOB [Bits]	~ 7.5
Gain Error [%]	~ 30
Input BW [kHz]	25
Digital I/O Levels [V]	$0 \rightarrow V_{DD}$
Cell size [$\mu\text{m} \times \mu\text{m}$]	$\sim 127 \times 64$
TSMC Process Node [nm]	65