NCDC

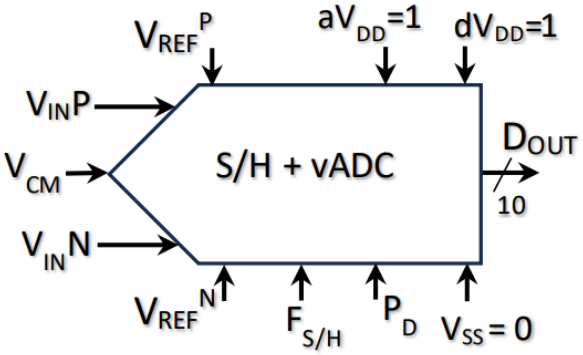
NUST CHIP DESIGN CENTRE

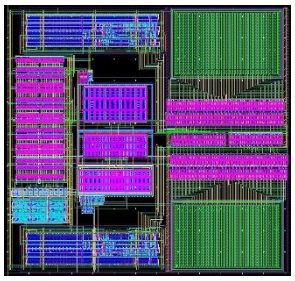
# Differential SAR-Based Voltage-Mode Synchronous ADC with S/H

## Overview

This IP is a low-power, 8-bit synchronous differential voltage ADC with integrated sample-and-hold and power-down features. It supports ~1 V peak-to-peak input swing around a 0.5×$V_{DD}$ common-mode voltage and includes an optional serialized digital output. The synchronous architecture enables dynamic reduction of digital power in steady-state conditions. Designed in 65 nm technology, it achieves ~7.1 ENOB with ~0.8 µA current consumption and a 25 kHz input bandwidth.

## Block Diagram



## Key Features

- 8-bit resolution, Low-Power, Differential voltage-input, Synchronous vADC with S/H & Power Down
- Optional: Digital output port ($D_{OUT}$) can be serialized as needed.
- Digital power consumption reduces dynamically in steady-state $V_{IN}$ conditions, enabled by synchronous vADC architecture.
- $V_{INP}$ and $V_{INN}$ terminals swing ~1V Peak-to-Peak around common mode voltage (e.g., $V_{CM}$ ≈0.5x$V_{DD}$)
- Example: $V_{REFP}$ ≈ 1v and $V_{REFN}$ ≈ 0v

## Applications

- Wearable devices
- Audio applications

## Specifications

| | |
|---|---|
| Resolution [Bits] | 8 |
| $V_{REF}$ P [v] | ~1 |
| $V_{REF}$ N [v] | 0 |
| $V_{CM}$ [v] | ~0.5 x $V_{DD}$ |
| $I_{DD}$ [µA] | ~0.8 |
| ENOB [Bits] | ~7.1 |
| Gain Error [%] | ~20 |
| Input BW [kHz] | 25 |
| Digital I/O Levels [v] | 0 → $V_{DD}$ |
| Cell size [µm X µm] | ~66x62 |
| TSMC Process Node [nm] | 65 |

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