NCDC
NUST CHIP DESIGN CENTRE

Differential SAR-Based Voltage-Mode Asynchronous ADC with S/H

Overview

This IP is a low-power, 10-bit asynchronous differential voltage ADC with integrated sample-and-hold and power-down features. It supports ~1 V peak-to-peak input swing around a $0.5 \times V_{DD}$ common-mode voltage and includes an optional serialized digital output. The asynchronous architecture enables dynamic reduction of digital power in steady-state conditions. Designed in 65 nm technology, it achieves ~9.2 ENOB with ~1.2 µA current consumption and a 15 kHz input bandwidth.
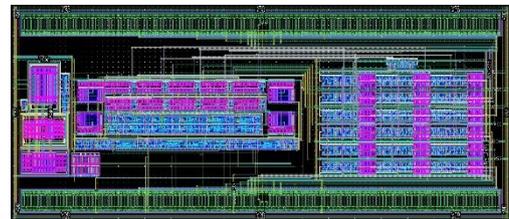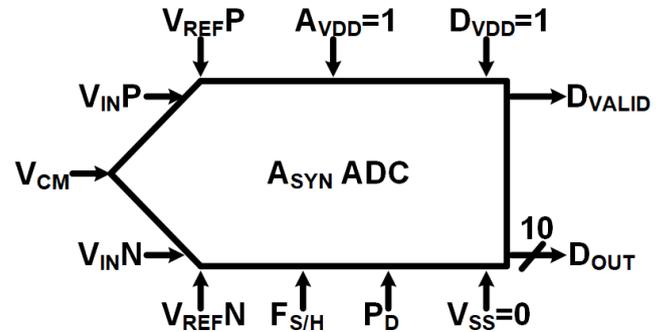
Key Features

- 10-bit resolution
- Low-Power
- Differential voltage-input
- Asynchronous ADC with S/H & Power-Down
- Digital output port (D_{OUT}) can be serialized as needed.
- $V_{IN}P$ and $V_{IN}N$ terminals swing ~1v Peak-to-Peak around common mode voltage (e.g., $V_{CM} \approx 0.5 \times V_{DD}$)

Applications

- Wearable devices
- Audio applications

Block Diagram

Specifications

Resolution [Bits]	10
$V_{REF}P$ [v]	~1
$V_{REF}N$ [v]	0
V_{CM} [v]	~0.5 x V_{DD}
I_{DD} [µA]	~1.2
ENOB [Bits]	~9.2
Gain Error [%]	~30
Input BW [kHz]	15
Digital I/O Levels [v]	0 → V_{DD}
Cell size [µm X µm]	~94x41
TSMC Process Node [nm]	65