NCDC

NUST CHIP DESIGN CENTRE

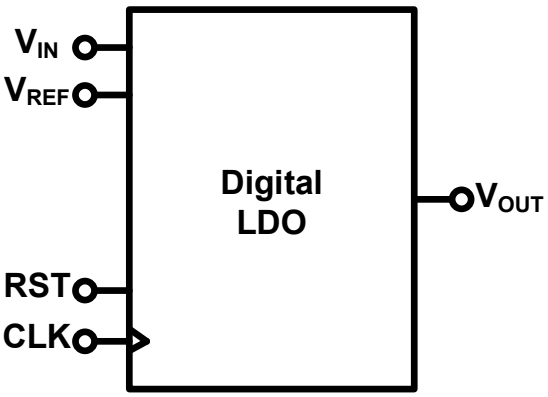
0.5-160mA, 20mV Dropout, Fast Transient Digital LDO

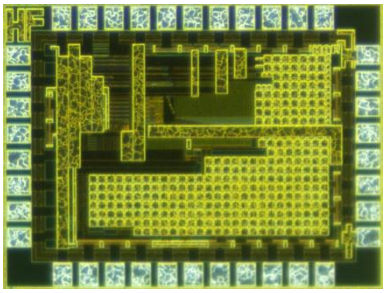
Overview

A digital low dropout (DLDO) regulator, with ≤0.13mV steady-state voltage ripples (V_{RIPP}) and a minimum dropout voltage of 20 mV, for driving both noise-sensitive analog and power-efficient digital load circuits in system-on-chip circuits.

The Silicon proven DLDO is designed in 180-nm CMOS process with a die area of 0.22 mm^2. The DLDO achieves a line regulation of 4 mV/V and a load regulation of 0.01 mV/mA while driving a maximum I_{LOAD} of 160 mA with a peak current efficiency of 99.96 %.

Block Diagram





Key Features

- Ripple-less output
- Fast transient
- Low dropout voltage
- Undershoot limiter
- Multi-bits shift handler
- High current and power efficiency
- Low quiescent current

Applications

- 0.5 – 160 mA load handler
- 0.88 – 1.7 mV On-Chip voltage reference

Specifications

Process [nm]	180
V_{IN} [V]	0.9 – 1.8
V_{OUT} [V]	0.88 – 1.7
V_{RIPP} [mV]	0.13
V_{DO} [V]	0.02
I_{LOAD} [mA]	0.5 – 160
I_Q [µA]	58
PSRR [dB]	-16 @ 1KHz
Load Reg. [mV/mA]	0.01
Line Reg. [mV/V]	4
Current efficiency [%]	99.96
Power Efficiency [%]	97.49
C_{OUT} [nF]	0.227

NCDC, National University of Sciences and Technology, SINES building, Sector H-12, Islamabad.

contact@ncdc.nust.edu.pk, www.ncdc.pk