

10 bits, Differential SAR-Based Voltage-Mode TSMC Cap DAC Asynchronous ADC with S/H

Overview

A 10-bit differential SAR-based voltage-mode Asynchronous ADC with sample-and-hold (S/H) and power-down features, designed for low-power operation in a 65nm process. Supports differential inputs with a V_{INP}/V_{INN} swing of ~ 1 V around a common-mode voltage, delivers an ENOB of 9.7, and has a gain error of 30%. Operating with 15 KHz input bandwidth and quiescent current (I_{DD}) of $1.5 \mu\text{A}$, the design includes a serializable digital output port (D_{OUT}) with I/O levels from 0 to V_{DD} . The compact layout occupies $112 \times 101 \mu\text{m}^2$.

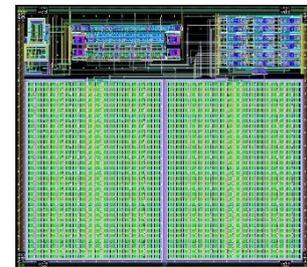
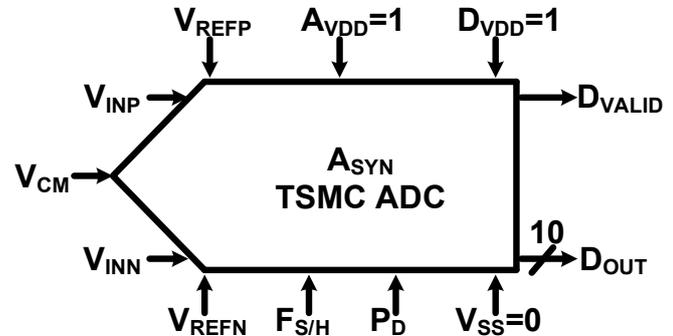
Key Features

- 10-bit Resolution
- Low-Power
- Differential voltage-input
- Asynchronous vADC with S/H & Power-Down
- Digital output port (D_{OUT}) can be serialized as needed
- Digital power cuts in steady-state, via async vADC
- V_{INP}/V_{INN} swing $\sim 1\text{V}$ around V_{CM} ($\sim 0.5 \times V_{DD}$).

Applications

- Wearable devices
- Audio applications

Block Diagram



Specifications

Process [nm]	65 LP
Resolution [Bits]	10
Differential V_{IN} p-to-p [V]	$0 \rightarrow V_{REF}$
I_{DD} [μA]	1.5
Power Consumption [μW]	≥ 2
ENOB [Bits]	9.7
Gain Error [%]	30
Input Bandwidth [KHz]	15
Digital I/O Levels [V]	$0 \rightarrow V_{DD}$
Area [$\mu\text{m} \times \mu\text{m}$]	112×101