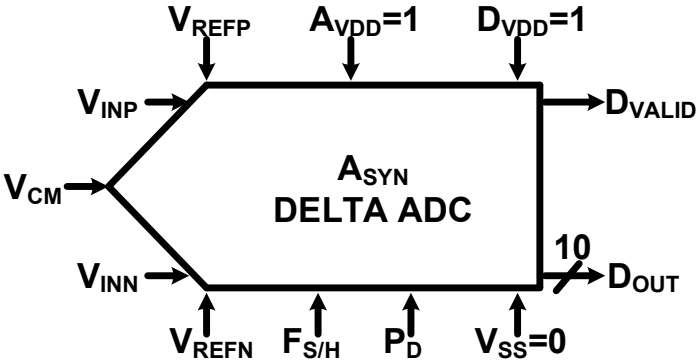
NCDC
NUST CHIP DESIGN CENTRE

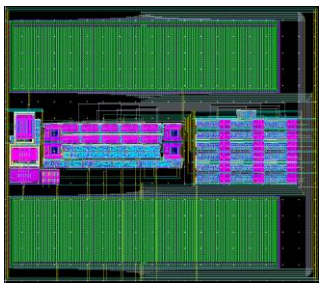
10 bits, Differential SAR-Based Voltage-Mode DELTA Cap DAC Asynchronous ADC with S/H

Overview

A 10-bit differential SAR-based voltage-mode Asynchronous ADC with sample-and-hold (S/H) and power-down features, designed for low-power operation in a 65nm process. Supports differential inputs with a V_{INP}/V_{INN} swing of ~1 V around a common-mode voltage, delivers an ENOB of 9.1, and has a gain error of 20%. Operating with quiescent current (I_{DD}) of 1 µA, the design includes a serializable digital output port (D_{OUT}) with I/O levels from 0 to V_{DD}. The compact layout occupies 96 x 84 µm^2.

Block Diagram





Key Features

- 10-bit Resolution
- Low-Power
- Differential voltage-input
- Asynchronous vADC with S/H & Power-Down
- Digital output port (D_{OUT}) can be serialized as needed
- Digital power cuts in steady-state, via async vADC
- V_{INP}/V_{INN} swing ~1V around VCM (~0.5×V_{DD}).

Applications

- Low power audio application
- Wearable devices

Specifications

Process [nm]	65 LP
Resolution [Bits]	10
Differential V_{IN} p-to-p [V]	0 → V_{REF}
I_{DD} [µA]	1
Power Consumption [µW]	≥2
ENOB [Bits]	9.1
Gain Error [%]	20
Digital I/O Levels [V]	0 → V_{DD}
Area [µm x µm]	96 x 84

NCDC, National University of Sciences and Technology, SINES building, Sector H-12, Islamabad.

contact@ncdc.nust.edu.pk, www.ncdc.pk