NCDC
NUST CHIP DESIGN CENTRE

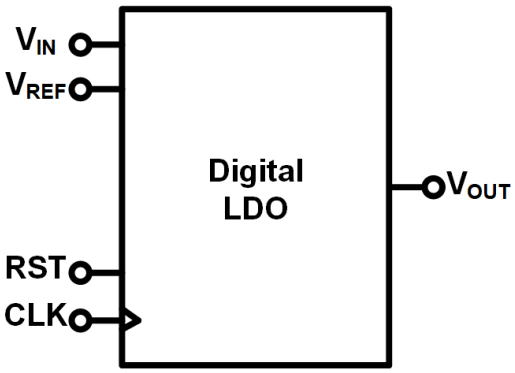
1-75mA, 20mV Dropout, Analog-Assisted Fast Transient Digital LDO

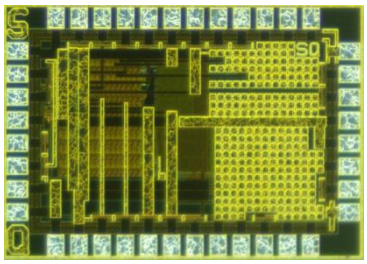
Overview

A digital low dropout (DLDO) regulator, with <0.14mV steady-state voltage ripples (V_{RIPP}) and a minimum dropout voltage of 20 mV, for driving both noise-sensitive analog and power-efficient digital load circuits in system-on-chip circuits.

The Silicon proven DLDO is designed in 180-nm CMOS process with a die area of 0.253 mm^2. The DLDO achieves a line regulation of 8 mV/V and a load regulation of 0.081 mV/mA while driving a maximum I_{LOAD} of 75 mA with a peak current efficiency of 99.93 %.

Block Diagram





Key Features

- Low noise
- Fast transient
- Low dropout
- Undershoot limiter
- Dual edge triggered shift register
- On-Chip load for calibration

Specifications

V_{DD} [V]	0.9 –1.8
V_{OUT} [V]	0.88 – 1.70
V_{RIPP} [mV]	0.14
V_{DO} [V]	0.02 – 0.1
I_{LOAD} [mA]	1 - 75
PSRR [dB]@1KHz	-30
Load Reg. [mV/mA]	0.081
Current efficiency [%]	99.93
Power Efficiency [%]	93.38
C_{OUT} [nF]	0.19

Applications

- 1 – 75 mA load handler
- 0.9 – 1.78 mV On-Chip voltage reference

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