NCDC
NUST CHIP DESIGN CENTRE

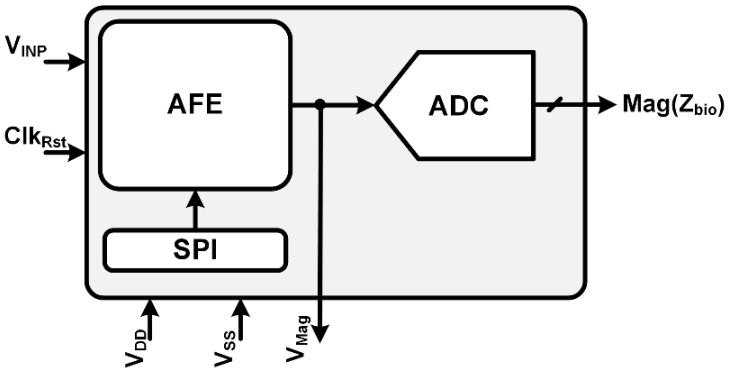
100 kS/s, Baseline-Canceling, Peak-Based Impedance Measurement IC for EIT

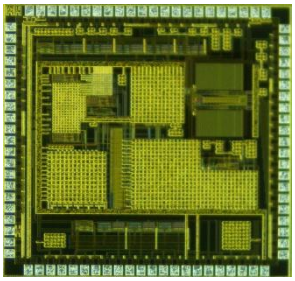
Overview

A high-throughput impedance measurement IC with <0.1% baseline resolution and 100 kS/s frame rate, designed for neural Electrical Impedance Tomography (EIT) applications.

The IC features a baseline-canceling peak detector that resets each cycle to a known DC level, enabling accurate extraction of small impedance changes riding on large signal baselines. Fabricated in a 180-nm CMOS process, the design supports a frequency range of 100 Hz to 100 kHz while consuming only 31–39 µW from a 1.2 V supply. The compact IC achieves a die area of 3.182 mm².

Block Diagram





Key Features

- High Throughput
- Baseline-Canceling Architecture
- High Sensitivity
- Low Power Consumption
- Scalable Architecture

Specifications

Process [nm]	180
V_{DD} [V]	1.2
Power [µW]	31 – 39
Frequency Range [Hz]	100 – 100k
Stimulus Current [µA]	10 – 100
Impedance Range [Ω]	10 – 30k
Throughput [S/s]	100 – 100k
Throughput / F.R. [S/s^2]	1
Chip Area [mm^2]	3.812

Applications

- Neural EIT
- Lung Ventilation Monitoring
- Breast Cancer Monitoring
- Cardiac Activities Monitoring

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