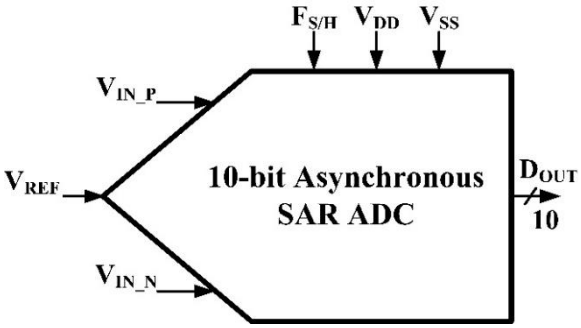
NCDC
NUST CHIP DESIGN CENTRE

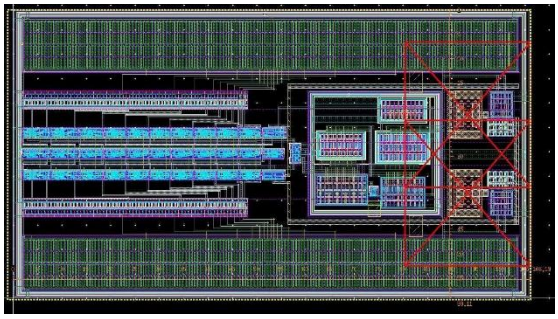
10-bit SAR ADC, 9.68 ENOB, 100MS/s, Compact and Low-Power SAR ADC

Overview

This 10-bit Successive Approximation Register (SAR) ADC is optimized for low power consumption and high-speed operation, achieving an effective number of bits (ENOB) of 9.68 at a sampling rate of 100 MS/s. Designed using a 65-nm CMOS technology, the ADC occupies a compact active area of just 0.0062 mm². It utilizes a minimal sampling capacitance of 1.04 pF, contributing to its energy efficiency. The total power consumption is remarkably low at 0.746 mW while maintaining high-speed performance at 100 MS/s.

Block Diagram





Key Features

- Low power
- High speed
- Compact Area
- Low sampling capacitance
- High SNR
- High ENOB

Applications

- Wireless communication
- Data acquisition systems

Specifications

Technology	65nm	
Supply Voltage [V]	1	1.2
Sampling Rate [MS/s]	50	100
Resolution [Bits]	10	
Sampling Capacitance [pF]	1.04	
ENOB [Bit]	9.51	9.68
Power [mW]	0.255	0.746
Area [mm^2]	0.0062	
SNR [dB]	57.35	60.03
Input Range V_{p-p}[V]	0.8	1.1

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